AMENDMENTS TO THE SPECIFICATION

Applicants respectfully present the following marked up replacement paragraph for consideration.

Replacement paragraph for page 14, lines 11-24.

When the interface cable is connected, the disconnection signal 'Select' become LO level and the PLL circuit 38 is activated and the counter 44 starts counting the leading edges of the quartz clock X'tal. And after a set number, it set the output CO to ~~HI~~ LO level and sets the internal connection signal CLKSEL to ~~HI~~ LO level. At that time the PLL circuit outputs the steady high-speed second clock PLL. On the other hand, when the interface is disconnected, the disconnection signal 'Select' becomes HI level, the PLL circuit is deactivated and stops the generation of the second clock PLL. Also, the counter 44 is preset by way of a NOR gate 46, and the output CO, as well as the internal disconnection signal CLKSEL, become HI level.

Replacement paragraph for the Abstract

One aspect of the present invention is a clock switching circuit for switching between asynchronous first clock and second clock when connecting or disconnecting an interface cable having a hot-plug function. ~~,and comprising:~~ The clock switching circuit includes a first group of flip-flops for receiving an interface disconnection signal that corresponds to disconnection and connection of the interface cable in response to the first clock[[;]], and a second group of flip-flops for receiving the interface disconnection signal in response to the second clock. ~~Furthermore, in this invention, as for the first flip-flops group, the flip-flop of the final stage thereof outputs a first selection signal through the first clock edges whose number is the stage number of the first flip-flop group, when the interface cable is disconnected; and the flip-flop of the final stage thereof outputs a first no-selection signal through one clock edge when the interface cable is connected. Also, the first clock is selected and output in response to the first selection signal, and the output of the first clock is prohibited in response to the first no-selection signal. Moreover, as for the second flip-flop group, the flip-flop of the final stage thereof outputs a second selection signal through the second clock edges whose number is the stage number of the second flip-flop group, when the interface cable is connected; and the flip-flop of the final stage thereof outputs a second no-selection signal through one clock edge when the interface cable is disconnected. The second clock is selected and output in response to the second selection signal, and the output of the second clock is prohibited in response to the second no-selection signal. In this invention, the second flip-flop group has more stages than the first flip-flop group by an amount that corresponds to the relationship between the frequency of the first and second clocks.~~